Digital Zero-Crossing Distortion in CCM Totem-Pole PFC: A Mechanism-Oriented Analysis

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1. Why the Zero Crossing?

- In CCM totem-pole PFC, the inductor current must track a sinusoid and pass smoothly through zero at every line-voltage reversal.
- High-frequency digital implementations show a localized current spike there, from digital timing, LF-leg commutation and DPWM limits acting on a non-ideal power stage.
- Near the crossing the required average inductor voltage is tiny, so a brief wrong-voltage interval costs a large current error.

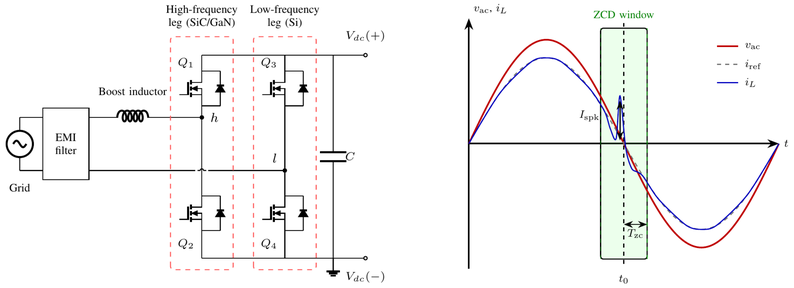


Fig. 1. (a) Totem-pole bridgeless PFC: SiC/GaN high-frequency leg, Si low-frequency leg. (b) ZCD window of $\pm T_{zc}$ around the reconstructed grid-voltage zero t_0.

Volt-second sensitivity

$$\Delta i_{\mathrm{err}} \approx (V_{\mathrm{err}}/L) \cdot \Delta t$$

A crossing error is a timing, modulation-realizability and sequencing problem, not only a current-loop compensation problem.

7.0 A

current error from a 10 µs unintended interval (V_{err} = 400 V, L = 572 µH)

Four Recurring Gaps in Reported Work

Baseline attribution
Gains rarely isolated on the same plant, controller, sensing chain and operating point.

Localized metrology
Full-cycle THD can't separate spike size, recovery time and deliberate dead zones.

Architecture portability
Many fixes need signed control quantities; transfer to rectified control is unclear.

System-level cost
Current-quality gains seldom reported with switching, recovery, EMI or auxiliary penalties.

2. Six Mechanism Clusters

M1 — HF-leg duty exchange & DPWM realizability
Duty swings between ~0 % and ~100 %; minimum-pulse limits and N-bit quantization create bridge-voltage error.
Observe: HF duty command, realized gate pulses

M2 — LF-leg commutation & device transitions
Low current slows C_{oss} charging; Si body-diode recovery injects current; early HF restart applies a wrong voltage.
Observe: LF midpoint voltage, commutation timing

M3 — Commutation-reference error & latency
Filtering, ADC, PLL, compute, PWM update and gate delay mistime polarity: $t_{delay} = V_{offset} / (R_s G|di_L/dt|)$.
Observe: LF midpoint voltage, commutation timing

M4 — Finite current-loop bandwidth
A band-limited loop creates leading input admittance, distorting the crossover even with perfect timing.
Observe: reference-to-current phase error

M5 — Input-filter current & measurement point
X-capacitor current ($\approx \omega C_X V_{ac}$) shifts the grid-current zero; inductor and grid current differ near crossing.
Observe: inductor and grid current together

M6 — Near-crossing DCM & SR policy
CCM model fails in DCM; complementary SR conducts reverse current; loop-polarity or integrator state causes restart spikes.
Observe: signed current + SR device state

Red: event-localized, strongest during the reversal.
Blue: distributed over the line cycle, most visible at the crossing.

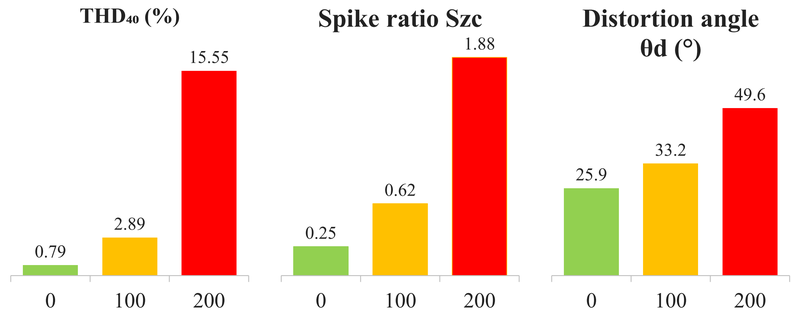
3. Crossing-Localized Metrics

Reported together as a vector: no single scalar captures ZCD severity.

THD_{40}	Harmonic content, h = 2–40
DF, D_{res}	All nonfundamental current in the acquisition band
S_{zc}	Peak deviation from the fundamental within $\pm T_{zc}$, per $\hat{I}_1$
θ_d	Recovery angle until error stays within 10 % of $\hat{I}_1$
Dead zone	Interval with $\lvert i_L \rvert$ < 5 %: exposes blanking trade-offs

4. Sensitivity to Polarity-Path Delay

Fixed 1 kW switched bench: 208 V_{rms}, 60 Hz → 400 V, f_{sw} = 100 kHz, L = 572 µH, rectified average-current control. Only the digital path is varied



Added polarity-path delay (µs), on top of the common 50 µs voltage-path delay. Every metric degrades steadily as delay grows.

THD_{40} understates broadband content
All non-idealities on: THD_{40} = 17.36 %, but DF = 0.8564 implies a residual of **60.3 %**.

Lower THD_{40} ≠ smaller spike
A 50 µs voltage delay drops THD_{40} from 1.24 % to 0.79 %, yet S_{zc} is unchanged and θ_d grows: a displacement correction only.

5. Eight Mitigation Families

Family	Targets	Principal limitation
A Blanking / soft-start	M1, M2, M6	Dead zone, restart distortion
B LF timing / DPWM	M1–M3	Modulation & switching complexity
C Duty feedforward	M4, M6	Model & transition sensitivity
D Admittance feedforward	M4, M5	Parameter dependence
E Commutation source	M3	Rectified-control portability
F Advanced current loop	M4	Computation & retuning
G Mode / SR management	M6	Diode conduction, state logic
H Auxiliary / soft transition	M2	Cost, redesign, mode change

6. Conclusion

The families act at different points of the crossing event, so practical designs layer them rather than pick one. Comparisons need a frozen baseline, localized metrics, the timing budget and the measurement point.